AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A method for using electrostatic forces to align semiconductor chips relative to each other, comprising:

electrically charging a first set of conductors on a first chip;

electrically charging a second set of conductors on a second chip;

placing the first chip face-to-face with the second chip, so that the first set of conductors is in close proximity to the second set of conductors; and

allowing electrostatic forces between the first set of conductors and the second set of conductors to bring the first chip into alignment with the second chip.

2. (Original) The method of claim 1, wherein the process of electrically charging the first set of conductors and the second set of conductors takes place after the first chip is placed face-to-face with the second chip.

3. (Original) The method of claim 1, wherein the process of electrically charging the first set of conductors and the second set of conductors involves applying a changing pattern of voltages to the first set of conductors and the second set of conductors.

4. (Original) The method of claim 1, further comprising vibrating the first chip and/or the second chip to facilitate aligning the first chip and the second chip.

5. (Original) The method of claim 1, further comprising applying a lubricant between the first chip and the second chip to reduce frictional forces between the first chip and the second chip during the alignment process.

6. (Original) The method of claim 1, wherein placing the first chip face-to-face with the second chip involves using a mold as a guide to facilitate bringing the first set of conductors in close proximity to the second set of conductors.

7. (Original) The method of claim 1, wherein a pattern formed by the first set of conductors matches a pattern formed by the second set of conductors.

8. (Original) The method of claim 1, wherein the first set of conductors and the second set of conductors are arranged in a checkerboard pattern.

9. (Original) The method of claim 1, wherein the first set of conductors and the second set of conductors are arranged in a pattern of concentric circles.

10. (Original) The method of claim 1, wherein the first set of conductors and the second set of conductors are arranged in a pattern with an autocorrelation approaching an impulse.

11. (Original) The method of claim 1, wherein the electrostatic forces between the first set of conductors and the second set of conductors include attractive forces and/or repulsive forces.

12. (Original) The method of claim 11, wherein the electrostatic forces between the first set of conductors and the second set of conductors generate a net

repulsive force that levitates the first chip over the second chip, thereby reducing frictional forces between the first chip and the second chip.

13. (Original) The method of claim 1, wherein the first set of conductors comprises part of a power network and/or a ground network of the first chip.

14. (Original) The method of claim 1, wherein electrically charging the first set of conductors on the first chip involves charging different conductors to different voltage levels.

15. (Original) The method of claim 1, wherein electrically charging the first set of conductors involves using electron-implanted charges.

16. (Original) The method of claim 1, further comprising bonding the first chip with the second chip after the first chip is brought into alignment with the second chip.

17-33. (Canceled).